SCHEME AND SYLLABUS

Doctor of Philosophy
in
Electronics Engineering

(w.e.f. Session Oct-2024)

DEPARTMENT OF ENGINEERING AND TECHNOLOGY

Gurugram University, Gurugram, Haryana

Ph.D. Course work guidelines

As per UGC Regulations 2016: Minimum Standards and procedure for Award of Ph.D. Degree, after admission in Ph.D., a research scholar shall be required to undertake course work for a minimum period of one semester.

COURSE STRUCTURE:

Subject Code	Name of course	Credits	Marks		
			External	Internal	Total
	RESEARCH METHODOLOGY	4	70	30	100
	RESEARCH AND PUBLICATION ETHICS	2	35	15	50
	SUBJECT SPECIFIC	4	70	30	100
	SEMINAR	4	--	100	100
Total		**14**	175	175	350

All scholar enrolled in the course work must choose one subject-specific course must be from the Subject-Specific Course List provided by the department.

Department of Engineering & Technology
Gurugram University, Gurugram

Ph.D. Coursework Syllabus- Oct-2024 onwards

Research and Publication Ethics (RPE)

Course Id: 24/PHD/COM01:

Total Marks : 50 (External = 35 Marks + Internal = 15 Marks) Credit : 02 (30 hrs)

Overview: This course as total 6 units focusing on basic of philosophy of science and ethics. Research integrity, publication ethics. Hands-on-sessions are designed to identify research misconduct and predatory publications. Indexing and citation databases, open access publications, research metrics (citations, h-index, impact factor, etc.) and plagiarism tools will be introduced in this course.

Pedagogy: Classroom teaching, guest lectures, group discussion and practical sessions.

Learning Outcome

By the end of the course, students will be able to understand the importance of being ethical in carrying out research and publication activities. They will be able to differentiate the quality publication practices and how to cognisant about dubious publishing practices/publishers. More importantly, there will be an increased awareness about 'open access' and contribution of research output to open access publishing platforms. The learners will also get acquainted with the software/databases which are necessary for carrying out research work.

Detailed Syllabus

Instructions for q.paper setter:

The question paper shall comprise eight questions of Seven Marks each (at least one questions from each unit). The students will be required to attempt five questions.

The internal assessment will be done through tutorials, assignments, quizzes and Group discussion. Weightage will be given for active participation.

Unit 1: Philosophy and Ethics (3hrs)

1. Introduction to philosophy: definition, nature and scope, concept, branches
2. Ethics: definition, moral philosophy, nature of moral judgments and reactions.

Unit 2: Scientific Conduct (5 hrs)

1. Ethics with respect to science and research
2. Intellectual honest and research integrity
3. Scientific misconducts: falsification, fabrication, and plagiarism
4. Redundant publications: duplicate and overlapping publications, salami slicing

5. Selective reporting and misrepresentation of data

Unit 3: Publication Ethics (7 hrs)

1. Publication ethics: definition, introduction and importance
2. Best practices/standard setting initiatives and guidelines: COPE, WAME, etc.
3. Conflictes of interest
4. Publication misconduct: deifinition, concept, problems that lead to unethical behavior and vice verse, types
5. Violation of publication ethics, authorship and contributor ship
6. Identification of publication misconduct, complaints and appeals
7. Predatory publishers and journals

PRACTICE:

Unit 4: Open Access Publishing (4hrs)

1. Open access publications and initiatives
2. SHERPA/RoMEO online resource to check publisher copyright and self-archiving policies.
3. Software tool to identify predatory publications developed by SPPU
4. Journal finder/journal suggestion tool viz. JANE, Elsevier Journal Finder, Springer Journal Suggested, etc.

Unit 5: Publication Misconduct (4 hrs)

A. Group Discussions (2hrs)
   1. Subject specific ethical issues, FFP, authorship
   2. Conflicts of interest
   3. Complaints and appeals: examples and fraud from India and abroad

B. Software Tools (2hrs):
   1. Use of plagiarism software like Turnitin, Urkund and other open source software tools.

Unit 6: Databases and Research Metrics (7hrs)

A. Databases (4hrs)
   1. Indexing databases
   2. Citation databases: Web of Science, Scopus, etc.

B. Research Metrics (3hrs)
   1. Impact Factor of journal citation report, SNIP, SJR, IPP, Cite Score
   2. Metrics : h-index, g index, i10 index, altmetrics.

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Ph.D. Coursework Syllabus- Oct-2024 onwards

RESEARCH METHODOLOGY

Total Marks: 100 (External =70 Marks + Internal =30 Marks) **Credit: 4**

Exam Time: 3Hours

OBJECTIVES

The course objectives are:

- **To introduce the fundamental concepts and scope of research**, including its objectives, characteristics, types, and the systematic process involved in formulating a research problem and hypothesis.
- **To design effective research methodologies**, including variable identification, instrument construction, sampling techniques, and data collection methods with attention to validity and reliability.
- **To develop analytical skills for data processing and interpretation**, using statistical techniques and software tools for both qualitative and quantitative research.
- **To equip students with academic writing and documentation skills**, emphasizing ethical practices, technical report writing, and the use of LaTeX for preparing research papers and theses.

LEARNING OUTCOMES

- Identify and explain the fundamental principles of research, including types, processes, and characteristics, as well as the formulation of research problems and hypotheses.
- Design and validate appropriate research instruments (e.g., questionnaires, scales) and select suitable data collection and sampling techniques based on research objectives.
- Perform and interpret statistical data analysis using tools such as Excel or statistical software, applying univariate to multivariate techniques appropriately.
- Produce well-structured research reports or theses using LaTeX, adhering to academic writing standards, ethical guidelines, and proper documentation methods.

COURSE OUTCOMES

Upon Completing the Course, Students will able:

CO1: **Describe** the fundamental concepts, types, and components of research, including the research process, characteristics of good research, and formulation of research problems and hypotheses.

CO2: **Classify and differentiate** among various research types and methodologies and evaluate appropriate use-cases for each.

CO3: **Develop and design** research instruments such as questionnaires and scales by applying principles of measurement, validity, and reliability, along with appropriate sampling and data collection methods.

CO4: **Analyze** research data using univariate, bivariate, and multivariate statistical techniques and interpret outputs from tools such as Excel and statistical software.

CO5: **Formulate and write** a structured research report or thesis by applying principles of technical writing, audience engagement, and ethical standards in research.

CO6: **Utilize** LaTeX for academic writing, including formatting research papers and theses, while understanding its significance in scholarly communication and reproducibility.

SYLLABUS

Unit I

Meaning, objectives and motivations in research, Characteristics and limitations of research, Components of research work, Criteria of good research, Research process, Types of Research, Fundamental, Pure or Theoretical Research, Applied Research, Descriptive Research, Evaluation Research, Experimental Research, Survey Research, Qualitative Research, Quantitative Research, Historical Research; Research problem: Selecting and analyzing the research problem, problem statement formulation, formulation of hypothesis, Literature review: purpose, sources, and importance - literature review procedure. Objectives: Learning Objectives; Definitions; Formulation of the research objectives.

Unit II

Variables in Research, Measurement and scaling, Different scales, Construction of instrument, Validity and Reliability of instrument. Data Collection methods: primary and secondary data, Construction of questionnaire and instrument, validation of instruments. Sample size determination, Sample design and sampling techniques. Processing of Data: Editing of Data, Coding of Data, Classification of Data, Statistical Series.

Unit III

Qualitative vs Quantitative data analyses: Univariate, Bivariate and Multivariate statistical techniques, Introduction to Excel, Data handling and plotting in Excel, Plotting software (at least one), Measures of Central Tendency, Dispersion, correlation and Regression, Chi-square test: Applications, Steps, characteristics, limitations, Analysis of Variance and Covariance, Factor analysis, Discriminant analysis, cluster analysis, multiple regression and correlation, multidimensional scaling, Conjoint Analysis, Application of statistical software for data analysis.

Unit IV

Research report: Different types, Contents of report, executive summary, contents of chapter, report writing, the role of audience, readability, comprehension, tone, final proof, report format, title of the report, Ethical issues in research: Code of Ethics in Research: Ethics and Research Process, Importance of Ethics in Research; Formal Methods: Formal Specification, Algorithm, and Complexity; Building Artefacts: Proof of Performance, Proof of Concept, and Proof of Existence; Process Methodology: Methods for Software Engineering and Human-Computer Interaction, Cognitive Processes, Interactive Games, Social Networks, and Web Analytics.

Introduction to Latex, Elementary Latex syntax, Paper and thesis writing using Latex

TEXTBOOKS

1. **Kothari, C. R., & Garg, G.** *Research Methodology: Methods and Techniques* (4th Edition), New Age International Publishers
2. **Creswell, J. W.** *Research Design: Qualitative, Quantitative, and Mixed Methods Approaches* (5th Edition), SAGE Publications
3. **Cooper, D. R., & Schindler, P. S.** *Business Research Methods* (12th Edition), McGraw-Hill Education
4. **Saunders, M., Lewis, P., & Thornhill, A.** *Research Methods for Business Students* (7th Edition), Pearson Education
5. **Leedy, P. D., & Ormrod, J. E.** *Practical Research: Planning and Design* (12th Edition), Pearson

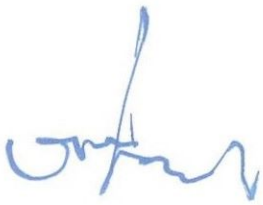
REFERENCE BOOKS

1. **Montgomery, D. C., & Runger, G. C.** *Applied Statistics and Probability for Engineers,* Wiley
2. **Trochim, W. M. K.** *Research Methods: The Essential Knowledge Base,* Cengage Learning
3. **Best, J. W., & Kahn, J. V.** *Research in Education,* Pearson
4. **Bell, J.** *Doing Your Research Project: A Guide for First-Time Researchers,* McGraw-Hill Education
5. **Lamport, L.** *LaTeX: A Document Preparation System,* Addison-Wesley

RELEVANT MOOC/SWAYAM/NPTEL COURSES:

1. **Research Methodology** – by Prof. A. K. Tripathi (IIT Roorkee) https://nptel.ac.in/courses/121105007
2. **Data Analysis and Decision Making** – by Prof. G. Srinivasan (IIT Madras) https://nptel.ac.in/courses/110106064
3. **Technical Writing** – by Prof. S. S. Dash (IIT Madras) https://nptel.ac.in/courses/109106094

Paper Setting Instruction: The examiner will set nine questions in total. The students have to attempt five questions in total, the first being compulsory and selecting one from each unit. Question one will have seven parts from all units and the marks of first question will be of 14 (1Q * 2 Marks). The remaining eight questions to be set by taking two questions from each unit and the marks of each question 14.



SUBJECT SPECIFIC COURSE:

S.No	Subject Code	Name of Subject
1		Hardware and Software Co-design of Embedded Systems
2		Device Modeling
3		Analog IC Design
4		Physical Design Automation
5		FPGA Design
6		Nano-electronic Materials and Devices
7		Internet of Things (IoTs)
8		Deep Learning Architectures
9		Quantum Computing
10		Microchip Fabrication Techniques

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Ph.D. Coursework Syllabus- Oct-2024 onwards
Electronics Engineering

Hardware and Software Co-design of Embedded Systems

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04
Exam Time: 3Hours

Course Outcomes: At the end of the course, the student will be able to:

CO-1 Understand Hardware/Sc ftware Co-design

CO-2 Model the data flow and implement the same through software and hardware.

CO-3 Design the hardware controllers through Control Flow Graph Structures.

CO-4 Understand the design principles in SoC Architecture

CO-5 Design CORDIC and Crypto coprocessor architectures Course

Syllabus:

Unit I:

The Nature of Hardware and Software: Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design.

Data Flow Modeling and Transformation: Introducing Data Flow Graphs, Analyzing Synchronous Data Flow Graphs, Control Flow Modeling and the Limitations of Data Flow, Transformations.

Unit II:

Data Flow Implementation in Software and Hardware: Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow.

Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph, Construction of the Data Flow Graph.

Unit III:

Architectures for Embedded Systems: Single processor – coprocessor architecture, mixed-signal architectures, multiprocessor architectures, reconfigurable architectures, Systems on Chip. Performance

Modeling: System-level performance modeling vs. low-level performance modelling, Modeling of system latency, energy consumption etc for hardware and software, Estimation of memory requirements.

Unit IV: System-Level Synthesis and Trade-off Analysis: Design of customized digital blocks, Hardware/software partitioning. Task binding, IP core integration and communication synthesis: Hardware and software interface synthesis,

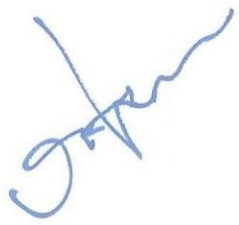
Hardware IP core synthesis: High-level synthesis: behavioral specification of hardware, module set allocation, resource binding, operation scheduling, controller design

Text Books:

1. Patrick Schaumont, A Practical Introduction to Hardware/Software Co-design, Springer, 2010.
2. A. Doboli, E. Currie, "Introduction to Mixed-Signal Embedded Design", Springer, 2010.
3. G. De Micheli, R. Ernst, W. Wolf, "Readings in Hardware/Software Co-Design", Morgan Kaufman, 2002.
4. Ralf Niemann, Hardware/Software Co-Design for Data flow Dominated Embedded Systems, Springer, 1998.

Paper Setting Instruction:

The examiner will set nine questions in total. The students have to attempt five questions in total, the first being compulsory and selecting one from each unit. Question one will have seven parts from all units and the marks of first question will be of 14 (1Q * 2 Marks). The remaining eight questions to be set by taking two questions from each unit and the marks of each question 14.



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Ph.D. Coursework Syllabus- Oct-2024 onwards
Electronics Engineering

Device Modelling

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04
Exam Time: 3Hours

Course Outcomes:

CO-1 Understand the governing equations along with their boundary conditions.

CO-2 Develop a sound physical and intuitive understanding of semiconductor devices

CO-3 Achieve ability to make key decisions while designing applications specific semiconductor devices.

CO-4 Simulate characteristics of a simple device using MATLAB, SPICE or other tools.

Syllabus:

Unit 1:

Introduction: significance of modelling Review of crystal structure: Unit cell and Miller Indices, Doping, Band Structure, Effective Mass, Density of states, Electron Mobility, Semiconductor Statistics- Fermi- Dirac function and carrier concentration calculation.

Semiclassical Transport Theory: Distribution Function, Boltzmann Transport Equation (BTE), Relaxation Time Approximation (RTA), Scattering and Mobility.

Unit II:

Drift-Diffusion (DD) model: Drift-Diffusion Model Derivation and dielectric relaxation time, Taylor series expansion and Finite Difference method, Normalization, Scaling and Linearization of Poisson's Equation and Scharfetter–Gummel Discretization of the Continuity Equation, Generation and Recombination models, Derivation of SRH model, Boundary conditions, Gummel's Iteration Method and Newton's Method, Drift Diffusion Application example.

Unit III:

Hydrodynamic Modelling: As extension of DD model, Carrier Balance, Energy balance and momentum balance Equations, Direct solution scheme through Monte Carlo simulations

Quantum Transport models: Tunneling, Schrodinger equation and free particle, potential step, potential barrier, Transfer Matrix Approach, Quantum Mechanical corrections to standard approach.

Unit IV: Models for DD, Hydrodynamic simulations, Mobility and G-R models, Selected Examples: SPICE Diode and MOSFET Models and Their Parameters

Text Books:

1. Snowden, "Introduction to Semiconductor Device Modelling", World Scientific, 2011.
2. S. M. Sze and Kwok K. Ng, Physics of Semiconductor Devices, John Wiley & Sons, 2006, 3 rd Edition.
3. Mark Lundstrom, Fundamentals of Nanotransistors, World Scientific, 2017.
4. Yannis Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, Oxford University Press, 2011, 2 nd Edition.
5. Supriyo Datta, Lessons from Nanoelectronics: A New Perspective on Transport (In 2 Parts), World Scientific, 2018, 2nd Edition.
6. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995, 1st Edition.
7. N. Arora, MOSFET Models for VLSI Circuit Simulation: Theory and Practice, Springer-Verlag Wein New York, 1993.
8. Norman G. Einspruch and Gennady Gildenblat, Advanced MOS Device Physics, Academic Press, 1989.
9. Y. Leblebici and S. M. Kang, Hot-Carrier Reliability of MOS VLSI Circuits, Springer Science + Business Media, LLC, 1993.
10. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009

Other Suggested Readings:

NPTEL Courses (https://archive.nptel.ac.in/courses/108/105/108105188/)

Paper Setting Instruction:

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Electronics Engineering

Analog IC Design

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04
Exam Time: 3Hours

Course Outcomes:

CO-1 Understand the biasing styles and limitations
CO-2 Design CMOS analog basic building blocks
CO-3 Evaluate different CMOS amplifier topologies and design for given specifications
CO-4 Comprehend the stability issues of the systems and design two stage amplifier

Syllabus:

Unit 1: Review of MOSFET device characteristics: Second order effects, MOS small signal Model, Capacitances, body bias effect, Current biasing, voltage biasing, Technology biasing, Relative comparision and limitations

Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references, Mismatch inaccuracies, Design solutions to minimize mismatch inaccuracies.

Unit 1I: Single stage amplifier: Analytical justification of operating region suitable for amplification/switching , Design of CS amplifier with different loads, Limitations of diode connected load, Improving output impedance of CS amplifier through feedback ,small signal analyses of common gate and common drain topologies and their frequency response with parasitic affects, significance of cascode, design of cascode amplifier and with ideal current source load and practical cascode load, Limitations of cascode, folded cascode amplifier and design with parasitics.

Unit 1II: Differential amplifier: Significance of differential signaling, Limitations of quasi differential amplifier, Design of differential amplifier with current source load and diode connected load and small signal analyses, errors due to mismatch, replication principle, qualitative analysis, common mode response, gilbert cell, Common centroid layout.

Unit 1V: Operational amplifier: characterization, two stage OP amp, small signal analysis, Miller compensation, effect of RHP zero on stability, Lead compensation, constant gm biasing, design of biasing circuit independent of process and temperature variations.

Band Gap Reference: General considerations, Supply independent biasing, temperature-independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, curvature correction, Design of BGR under low voltage conditions.

Text Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, 2nd Edition.
2. Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley, 2024, 6th Edition.
3. Mohammed Ismail and Terri Fiez, Analog VLSI: Signal and Information Processing, McGrawHill, 1994.
4. Randall L. Geiger, Phillip E. Allen and Noel R. Strader, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 1989.
5. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, 2nd Edition.
6. Paul G. A. Jespers and Boris Murmann, Systematic Design of Analog CMOS Circuits, Cambridge University Press, 2017.

Other Suggested Readings:

NPTEL Courses (https://nptel.ac.in/courses/117101105)

Paper Setting Instruction:

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Ph.D. Coursework Syllabus- Oct-2024 onwards
Electronics Engineering

Physical Design Automation

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04
Exam Time: 3Hours

Course Outcomes:

CO-1 Understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology.

CO-2 Adapt the design algorithms to meet the critical design parameters.

CO-3 Learn various layout optimization techniques and map them to the algorithms.

CO-4 Develop proto-type EDA tool and test its efficacy.

Syllabus:

Unit 1: VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multichip modules.

Unit 1I: Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

Unit 1II: Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin-based methods, neighbor pointers, corner stitching, multi-layer operations.

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs.

Unit 1V: Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, Kluwer Academic, 1999, 3rd Edition.

2. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2022, 2nd Edition.
3. Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer, 2008.
4. Reference Books:
5. Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008, 1st Edition
6. Sabih H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2008, 2nd Edition.
7. Charles J. Alpert, Dinesh P. Mehta and Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2009.

Other Suggested Readings:

NPTEL Courses (https://archive.nptel.ac.in/courses/106/105/106105161/)

Paper Setting Instruction:

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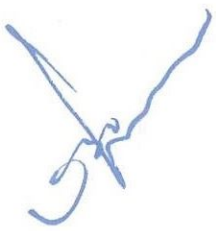

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Ph.D. Coursework Syllabus- Oct-2024 onwards
Electronics Engineering

FPGA Design

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04
Exam Time: 3Hours

Course Outcomes:

CO-1 Understand FPGA design flow.

CO-2 Identify the building blocks of commercially available FPGA/CPLDs.

CO-3 Develop VHDL/Verilog models and synthesize targeting for Vertex, Spartan FPGAs.

CO-4 Develop parameterized library cells & implement system designs

Syllabus:

Unit 1: Introduction to FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA.

Design Examples using PLDs Design of Universal block, Memory, Floating point multiplier, Barrel shifter.

Unit 1I: FPGAs/CPLDs: Programming Technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FPGA/CPLD.

Unit 1II: Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.

Unit 1V: Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures. FPGA architectural assumpticns, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA

CASE STUDY – Applications using Kintex-7, Viretex-7, Artix-7.

Text Books:

1. John V. Oldfield and Richard C. Dorf, Field Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems, Wiley-Interscience, 1995, 1st Edition.

2. Frank Bruno, FPGA Programming for Beginners, Packt, 2021.
3. Frank Bruno and Guy Eschemann, The FPGA Programming Handbook, Packt, 2024, 2nd Edition.
4. Stephen D. Brown, Robert J. Francis, Jonathan Rose and Zvonko G. Vranesic, Field Programmable Gate Arrays, Springer Science Business Media, LLC, 1992, 1st Edition.
5. Clive Maxfield, The Design Warrior's Guide to FPGAs: Devices, Tools and Flows, Elsevier-Newnes, 2004.
6. Data sheets of Artix-7, Kintex-7, Virtex-7.

Other Suggested Readings:

NPTEL Courses (https://nptel.ac.in/courses/117108040)

Paper Setting Instruction:

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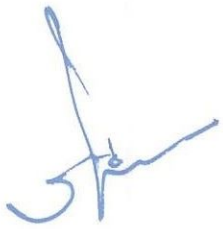

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Ph.D. Coursework Syllabus- Oct-2024 onwards
Electronics Engineering

Nano-electronic Materials and Devices

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04
Exam Time: 3Hours

Course Outcomes:

CO-1 Understand the physics and materials for Nanoelectronics

CO-2 Understand the scaling issues

CO-3 Explain the need for non-classical and non-silicon based devices

CO-4 Analyse the performance of novel devices

Syllabus:

Unit 1: Overview: Nano devices, Nano materials, Nano device characterization, Definition of Technology node, MOS capacitor, MOS Scaling theory, Moore's Law and Koomey's law.

Unit 1I: Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology, Role of interface quality and related process techniques, Gate oxide thickness, scaling trend, SiO2 vs High-k gate dielectrics, Integration issues of high-k, Interface states, bulk charge, band offset, stability, reliability - Qbd high field, possible candidates, CV and IV techniques, Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot, Metal gate transistor : Motivation, requirements, Integration Issues.

Unit 1II: Non-classical MOS transistor: Requirements, and Novel devices SOI - PDSOI and FDSOI, Ultrathin body SOI - double gate transistors, integration issues. Vertical transistors - FinFET and Cylindrical gate FET. Novel devices: Tunnel FET, Negative-Capacitance (NC) FET. Metal source/drain junctions - Properties of Schottky junctions on Silicon, Germanium and compound semiconductors -Workfunction pinning.

Unit 1V: Emerging Nano MOSFETs: strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors MOSFETs in the context of channel quantization and strain, Hetero structure MOSFETs, exploiting novel materials, strain, quantization. CNT, Graphene, Nanotubes, nanorods and other nano-structures.

Text Books:

1. Y. Taur and T. Ning, "Fundamentals of Modern VLSI devices" Cambridge University Press, 2022, 3rd Edition.

2. Nicollian and J. R. Brews "MOS (Metal Oxide Semiconductor) Physics and Technology" Wiley, 2002, 1st Edition
3. Brundle, C. Richard, Evans, Charles A. Jr., Wilson, Shaun "Encyclopedia of Materials Characterization", Butterworth-Heinemann Manning Publications Co., 1992,
4. Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017. 2nd Edtiton.
5. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009

Other Suggested Readings:

NPTEL Courses (https://archive.nptel.ac.in/courses/117/108/117108047/)

Paper Setting Instruction:

The examiner will set nine questions in total. The students have to attempt five questions in total, the first being compulsory and selecting one from each unit. Question one will have seven parts from all units and the marks of first question will be of 14 (1Q * 2 Marks). The remaining eight questions to be set by taking two questions from each unit and the marks of each question 14.

Department of Engineering & Technology
Gurugram University, Gurugram

Ph.D. Coursework Syllabus- Oct-2024 onwards
Electronics Engineering

Internet of Things (IoTs)

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04

Exam Time: 3Hours

Course Outcomes: At the end of successful completion of the course, students will be able to

CO1 Summarize the concepts of network connected embedded devices.

CO2 Design suitable network architecture and use appropriate protocols for a given IOT application.

CO3 Identify and summarize different components required for IOT applications.

CO4 Analyse the system through Data Analytics tools.

Syllabus:

Unit 1: Introduction & Basic of IoT: Definition, Characteristics, Physical and Logical Designs, challenges, Technological trends in IOT, IoT Examples, M2M

IoT: Communication and Networking Introduction to Sensing and Networking: Sensing & actuation, Wireless Senor network, Senor nodes, Communication Protocols, M2M Communication, Networking Hardware, Networking Protocols.

Unit 1I: IoT System Management: Network Operator Requirements, IoT Platform Design Specification – Requirements, Process, Domain Model, Service, IoT Level, Function, Operational view, Device and Component Integration, Application development. Infrastructure protocol (IPV4/V6/RPL), Identification (URIs), Transport (Wifi, Lifi, BLE), Discovery, Data Protocols, Device Management Protocols. – A Case Study with MQTT/CoAP usage-IoT privacy, security and vulnerability solutions.

Cloud Architecture Basics – Fundamentals of cloud, cloud architecture standards and interoperability- Cloud types; IaaS, PaaS, SaaS. Benefits and challenges of cloud computing, public, private clouds community cloud, Development environments for service development; Amazon, Azure, Google App cloud platform in industry

Unit 1II: Networking and Computing: File Handling, Python Packages for IoT, IoT Physical Servers – Cloud Storage Models, Communication APIs.

Role of Cloud Computing in IoT, AWS Components, Connecting a web application to AWS, IoT using MQTT, AWS IoT Examples. Security Concerns, Risk Issues, and Legal Aspects of Cloud Computing- Cloud Data Security

Unit 1V: IoT Clouds and Data Analytics: RESTful Web API, Amazon Web Services for IoT, Apache Hadoop, Batch Data Analysis, Chef, Chef Case Studies, Puppet, NETCONF-YANG.

Case studies with architectural analysis: IoT applications, Smart City, Smart Water, Smart Agriculture, Smart Energy, Smart Healthcare, Smart Transportation, Smart waste management

Text Books:

1. Kamal, R.,"Internet of Things – Architecture and Design Principles," 1st Edition, Mcgraw Hill,2017.
2. Simone Cirani," Internet of Things- Architectures, Protocols and Standards", WILEY,2018.
3. Alessandro Bassi," Enabling Things to Talk- Designing IoT solutions with the IoT Architectural Reference Model", Springer,2013.

Paper Setting Instruction:

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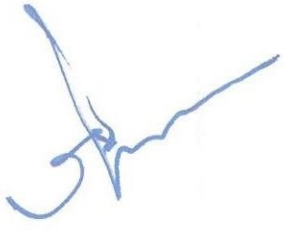

Department of Engineering & Technology
Gurugram University, Gurugram

Ph.D. Coursework Syllabus- Oct-2024 onwards
Computer Science and Engineering

Deep Learning Architectures

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04
Exam Time: 3Hours

Course Outcomes:

CO1 Understand the basic concepts of neural networks and deep learning methods

CO2 Know the basic model types used in deep learning, e.g., Convolutional Neural Networks (CNNs), Recurrent Neural Networks (RNNs), & Generative Adversarial Network (GANs)

CO3 Build and train deep neural networks and identify key architecture parameters

CO4 Modify state-of-the-art deep learning architectures for a new dataset/task. And re-train and tune hyper parameters of several classes of deep learning methods.

CO5 Know the suitability of specific deep learning methods to various real world data domains such as the ones arising from text, images, and videos.

Syllabus:

Unit 1: Introduction to Deep Learning: Neural Networks, The basic building blocks of deep learning, Training of Neural Networks.

Unit 1I: Convolutional Neural Networks (CNNs): CNN architectural details, CNN architectures – LeNet, AlexNet, VGG, Resenet, Googlenet, Inceptionnet. Training a CNNs: weights initialization, batch normalization, hyperparameter optimization, Understanding and visualizing CNNs.

Unit 1II: Recurrent Neural Networks (RNNs): RNNs, Need of RNN, The basic building blocks of RNNs and other architectural details, Study of some special RNN architectures: GRU, LSTM, Seq2Seq models, Attention mechanism.

Unsupervised deep learning: Self-organized maps,

Unit 1V: Autoencoders Generative models: Architectural and training of Generative Adversarial Networks (GANs), Restrictive Boltzmann Machines (RBMs), Stacking RBMs, Belief nets, Learning sigmoid belief nets, Deep belief nets Adversarial attacks on Neural Networks.

Text Books:

1. Ian Good fellow, Yoshua Bengio and Aaron Courville, Deep learning, In preparation for MIT Press, Available online: http://www.deeplearningbook.org, 2016

2. Satish Kumar, Neural Networks - A Class Room Approach, Second Edition, Tata McGraw-Hill, 2013.
3. Charu C. Aggarwal Neural Networks and Deep Learning Springer International Publishing, 2018
4. Andrew W. Trask, Grokking Deep Learning Manning Publications

Paper Setting Instruction:

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Ph.D. Coursework Syllabus- Oct-2024 onwards
Electronics Engineering

Quantum Computing

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks)

Credit: 04
Exam Time: 3Hours

Course Outcomes:

CO-1 Understand the principles of quantum computation qubit

CO-2 Analyze multi-qubit systems and protocols

CO-3 Apply quantum measurement and entanglement concepts

CO-4 Design and implement quantum algorithms and circuits

Syllabus:

Unit 1: Review of Quantum Mechanics and Motivation for Quantum Computation Qubit: The qubit state - matrix and Bloch sphere representation - computational basis unitary evolution.

Unit 1I: Multi-qubit states - No-cloning theorem - Superdense coding - Pure states to Bell states – Bell inequalities.

Protocols with multi-qubits: Swapping - Teleportation - gates: CNOT - Toffoli gate - NAND - FANOUT - Walsh Hadamard.

Unit 1II: Measurement: Projective operators - General, Projective and POVM measure, Ensemble: Density operators - pure and mixed ensemble - time evolution – post measurement density operator. Composite systems: Partial trace - Reduced density operator - Schmidt decomposition, Purification bipartite entanglement.

Unit 1V: Quantum computing: Classical computing using qubits - Quantum parallelism - Deutsch's algorithm -Deutsch Josza algorithm.

Quantum circuits: Basic gates - ABC decomposition - Gray codes - Universal gates - Principle of deferred and implicit measurements - Quantum Fourier transform - applications: phase estimation, order finding - factoring, discrete logarithm and hidden subgroup problems - Role of prime factoring in classical cryptography - search algorithms. Quantum error correcting codes, Physical realization of qubits.

Text Books:

1. M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2010, 10th Anniversary Edition

2. Chris Bernhardt, Quantum Computing for Everyone, The MIT Press, 2019.
3. Ray LaPierre, Introduction to Quantum Computing, Springer, 2021.
4. Quantum Theory: Concepts and Methods, Asher Peres, Kluwer Academic Publishers, 1993.
5. Venkateswaran Kasirajan, Fundamentals of Quantum Computing: Theory and Practice, Springer, 2021.

Other Suggested Readings:

NPTEL Courses (https://nptel.ac.in/courses/106106232)

Paper Setting Instruction:

The examiner will set nine questions in total. The students have to attempt five questions in total, the first being compulsory and selecting one from each unit. Question one will have seven parts from all units and the marks of first question will be of 14 (1Q * 2 Marks). The remaining eight questions to be set by taking two questions from each unit and the marks of each question 14.

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Ph.D. Coursework Syllabus- Oct-2024 onwards
Electronics Engineering

Microchip Fabrication Techniques

Total Marks: 100 (External = 70 Marks + Internal = 30 Marks) Credit: 04
Exam Time: 3Hours

Course Outcomes:

CO-1 Explain the unit fabrication process steps

CO-2 Analyze process yield and yield measurement for a process

CO-3 Propose the process flow for MOS devices

CO-4 Construct the circuit stick diagrams and circuit layout using the design rules

Syllabus:

Unit 1: Overview of semiconductor industry, unit process steps for fabrication

Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Contamination sources, Clean room construction;

Unit 1I: Oxidation: dry oxidation, wet oxidation; Photolithography: Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect.

Unit 1II: Etching: Dry etching, Wet etching, resist stripping; Doping: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2;

Deposition: CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapor phase epitaxy, molecular beam epitaxy; Chemical mechanical polishing; Metallization.

Unit 1V: Process flow for NMOS, PMOS, CMOS, BICMOS ICs, Novel MOS and GaN based devices.

Design rules, stick diagrams and layout.

Packaging: Chip characteristics, package functions, package operations

Yield Measurement: Types of Yields, Models, Effect of Contamination on Yield

Text Books:

1. Peter Van Zant, Microchip Fabrication, McGraw Hill, 2014, 6th Edition.
2. S.M. Sze, VLSI Technology, McGraw-Hill, 2017, 2nd Edition (Indian).

3. Sorab K Gandhi, VLSI Fabrication Principles: Silicon and Germanium Arsenide, Wiley, 1994, 2nd Edition.
4. James D Plummer, Peter B Griffin and Michael D Deal, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Pearson, 2009, 1st Edition.
5. Stephen A Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 2001, 2nd Edition.
6. C.Y. Chang and S.M. Sze, ULSI Technology, McGraw Hill, 2000, 2nd Edition

Other Suggested Readings:

NPTEL Courses (https://archive.nptel.ac.in/courses/108/108/108108113/)

Paper Setting Instruction:

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Department of Engineering & Technology
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Ph.D. Coursework Syllabus- Oct-2024 onwards
Seminar

Total Marks: 100 (Internal) Credit: 04

Objective:
The Seminar course aims to develop scholarly presentation skills, critical thinking, and familiarity with current research trends in the field of Computer Science and Engineering. Scholars are expected to explore, analyze, and present technical content from peer-reviewed sources and demonstrate command over their chosen topic.

Seminar Topics:
Topics must be research-oriented and aligned with the broad area of the scholar's Ph.D. thesis. The topic must be approved by the assigned faculty member within the first two weeks of the course.

Seminar Deliverables:
Each scholar must:

1. **Prepare a Seminar Report** (Approx. 15–20 pages) including:
   - Introduction and motivation
   - Literature survey
   - Problem definition or key research issues
   - Methodologies/technologies discussed
   - Summary and future scope
   - References (in IEEE format)
2. **Deliver an Oral Presentation** (Duration: 25–30 minutes):
   - Presentation should be prepared using PowerPoint or equivalent.
   - Question-and-answer session will follow.
3. **Submit a Plagiarism Report**:
   - Similarity index must be **below 10%**.
   - Plagiarism report (Turnitin/URKUND) must be submitted with the seminar report.

Evaluation Scheme : (Total Marks: 100) (Internal)

Component	Marks
Quality of Seminar Report	30
Depth of Literature Review	20
Content Delivery & Presentation	25
Response to Questions	15
Regularity and Participation	10
Total	**100**